

CLAIMS

1. (Presently amended) A method for varying the frame synchronization structure of an information stream, the method comprising:

providing selection bits;

receiving a first stream of information;

in response to the selection bits, selecting a first arrangement of synchronization bits in the first stream of information; and

in response to selecting the first arrangement of synchronization bits, synchronizing the first stream of information into a first frame structure.

2. (Previously presented) The method of claim 1 in which synchronization of the first stream of information includes:

reading the first arrangement of synchronization bits in the first stream of information; and

in response to reading the first arrangement of synchronization bits, organizing the first information stream into header and data sections.

3. (Original) The method of claim 2 in which the selection of the first arrangement of synchronization bits includes selecting a first arrangement of bits in the header section.

4. (Previously presented) The method of claim 2 in which the organization of the first stream of information into the first frame structure of header and data sections includes each header section having a plurality of m bits; and

in which the selection of the first arrangement of synchronization bits includes selecting a number of bits in the range from zero to m bits in the header section.

5. (Original) The method of claim 4 in which the selection of the first arrangement of synchronization bits includes selecting the bit position of each synchronization bit in the header section.

6. (Presently amended) The method of claim 5, further including providing content bits, in which the selection of the first arrangement of synchronization bits includes, in response to the content bits, selecting the content of the bits in the selected bit positions in the header section.

7. (Previously presented) The method of claim 2 further comprising:
deinterleaving the first stream of information into a plurality of n parallel data streams;

in which the organization of the first stream of information into the first frame structure includes each parallel data stream having a header and a data section; and

in which the selection of the first arrangement of synchronization bits includes selecting n arrangements of synchronization bits, one arrangement for each parallel data stream header section.

8. (Original) The method of claim 7 in which the selection of the first arrangement of synchronization bits in the header sections of the n parallel data streams includes selecting a unique arrangement of synchronization for each parallel data stream header section.

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9. (Previously presented) The method of claim 7 in which the deinterleaving of the first stream of information includes forming four parallel data streams; and

in which the reading of synchronization bits from the header sections of the parallel data streams includes reading a first group of synchronization bits from the first parallel data stream header section, a second group of synchronization bits from the second parallel data stream header section, a third group of synchronization bits from the third parallel data stream header section, and a fourth group of synchronization bits from the fourth parallel data stream header section.

10. (Original) The method of claim 9 in which the selection of the first arrangement of overhead bits includes:

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selecting a bit position for each of the first group of bits in the first header section;

selecting a bit position for each of the second group of bits in the second header section;

selecting a bit position for each of the third group of bits in the third header section; and

selecting a bit position for each of the fourth group of bits in the fourth header section.

11. (Original) The method of claim 10 in which the selection of the first arrangement of synchronization bits includes selecting the number of synchronization bits in the first, second, third, and fourth groups of synchronization bits.

12. (Previously presented) The method of claim 5 further comprising:
organizing a second stream of information in the first frame structure; and
selecting a second arrangement of synchronization bits to be written in the header section of the second stream of information.

13. (Original) The method of claim 12 further comprising:
transmitting the second stream of information with the second
arrangement of synchronization bits.

14. (Original) The method of claim 13 in which the second stream of
information is organized into a plurality of n parallel data streams;

in which the selection of the second arrangement of synchronization bits
includes writing n arrangements of synchronization bits, one arrangement for
each parallel data stream header sections; and

further comprising:

interleaving the n parallel data streams in to the second stream of
information.

[15 (first-occurring instance, Cancelled).]

15. (Original) The method of claim 1 in which the reception of the first
stream of information includes receiving the information in a protocol selected
from the group consisting of datacom, telecom, fiber channel, SONET, SDH, and
Gigabit Ethernet protocols.

16-18 (Cancelled).

19. (Original) A selectable frame synchronization structure transmission repeater comprising:

a repeater input port to accept a first stream of information including a first arrangement of synchronization bits; and

a decoder having a first input connected to the repeater input port to receive the first stream of information, the decoder reading the first arrangement of synchronization bits to organize the first stream of information into a first frame structure including a data section and a header section, the decoder having a second input for selecting the first arrangement of synchronization bits to be read.

20. (Original) The repeater of claim 19 in which the decoder synchronizes the first stream of information into the first frame structure including a header section having a plurality of m bits; and

in which the decoder selection of the first arrangement of overhead bits includes selecting a number of synchronization bits in the range from zero to m bits.

21. (Original) The repeater of claim 20 in which the decoder selection of the first arrangement of synchronization bits includes selecting the bit position of the synchronization bits in the header section.

22. (Original) The repeater of claim 21 in which the decoder selection of the first arrangement of synchronization bits includes selecting the content of each synchronization bit in the header section.

23. (Previously presented) The repeater of claim 22 further comprising:
a deinterleaver circuit having an input to receive the first stream of information, the deinterleaver circuit deinterleaving the first stream of information into a plurality of n parallel data streams; and

in which the decoder's first input includes a plurality of n inputs connected to the deinterleaver to receive the first stream of information in n parallel data streams, the decoder's selection of the first arrangement of synchronization bits includes selecting an arrangement of synchronization bits in each of the n parallel data streams to form a first frame structure including header and data sections in each data stream.

24. (Original) The repeater of claim 23 in which the decoder's selection of the first arrangement of overhead bits includes selecting independent arrangements of synchronization bits for each header section of the n parallel data streams.

25. (Previously presented) The repeater of claim 24 in which the deinterleaver circuit deinterleaves the first stream of [digital] information into four parallel data streams; and

in which the decoder's selection of the first arrangement of synchronization bits includes reading a first group of bits from the first parallel data stream header section, reading a second group of bits from the second parallel data stream header section, reading a third group of bits from the third parallel data stream header section, and reading a fourth group of bits from the fourth parallel data stream header section.

26. (Previously presented) The repeater of claim 22 further comprising:
an encoder having an output to provide a second stream of information organized in the first frame structure with header sections, the encoder having an input for selecting a second arrangement of synchronization bits to be written in the header section; and
a repeater output connected to the encoder output to provide the second stream of information.

27. (Original) The repeater of claim 26 in which the encoder organizes the second stream of information into a plurality of n parallel data streams, and in which the encoder selection of the second arrangement of synchronization bits includes selecting the synchronization bits to be written in the header sections of the n parallel data streams, the encoder having a plurality of n outputs to provide the n data streams; and

further comprising:

an interleaver circuit having a plurality of n inputs connected to n encoder outputs, the interleaver circuit interleaving the parallel data streams in to the second stream of information, the interleaver circuit having an output connected to the repeater output.

28. (Previously presented) The repeater of claim 19 in which the repeater input receives the first stream of information in a protocol selected from the group consisting of datacom, telecom, fiber channel, SONET, SDH, and Gigabit Ethernet protocols.

29. (Previously presented) A selectable frame synchronization structure communication system comprising:

a transmitter having an output to provide a first stream of information in a first frame structure with a header including a first arrangement of synchronization bits of the first stream of information;

a repeater including:

a repeater input port to accept the first stream of information; and

a decoder having a first input connected to the repeater input port to receive the first stream of information, the decoder reading the first arrangement of synchronization bits to organize the first stream of information into the first frame structure including a header section, the decoder having a second input to select the first arrangement of synchronization bits to be read.

B¹ anal. 30. (Original) The system of claim 29 in which the repeater further includes:

an encoder having an output to provide a second stream of information organized in the first frame structure with a header section, the encoder having an input for selecting a second arrangement of synchronization bits to be written in the header section; and

a repeater output connected to the encoder output to provide the second stream of information.

31. (Previously presented) The system of claim 30 further comprising:

a receiver having an input connected to the repeater output to accept the second stream of information, the receiver reading the second arrangement of synchronization bits to organize the second stream of information [stream] into the first frame structure.
